Fig. 4 is an exemplary plot of interference noise power integrated over the entire communications channel vs. distance from an intended subscriber using the same CDMA codes with different CDMA code lengths.

Fig. 5 is an exemplary plot of interference noise power integrated over the entire communications channel vs. distance from an intended subscriber using different CDMA codes and different CDMA code lengths.

Fig. 6 is an exemplary family of plot curves of ranging calibration data overhead vs. chip rate.

Fig. 7 is an exemplary family of plot curves of signal-to-noise ratio integrated over the entire communications channel vs. number of phase coherency bits.

Fig. 8 is an exemplary plot of Fourier processing overhead as a fraction of resource vs. data rate.

Fig. 9 is an exemplary flow chart 90 of a computer program for performing the coherent phase synchronization of the present invention.

Fig. 9A is a flow chart of step 906 in Fig. 9.

Fig. 9B is a flow chart of step 910 in Fig. 9.

Fig. 9C is a flow chart of step 914 in Fig. 9.

Fig. 10 is an embodiment of the present invention in a gateway 1000 for performing the functions in Fig. 9.

Description of the Invention

The following description is presented to disclose the currently known best mode for making and using the present invention. The scope of the invention is defined by the claims.

Fig. 1 is a diagram illustrating an exemplary multiple satellite communications system suitable for use with the present invention for coherent synchronization